

ABSTRACT

A memory architecture includes a first substrate containing multiple memory devices and a first channel portion extending across the first substrate. The architecture further includes a second substrate containing multiple memory devices and a second channel portion extending across the second substrate. A connector couples the first channel portion to the second channel portion to form a single channel. The connector includes a first slot that receives an edge of the first substrate and a second slot that receives an edge of the second substrate. Another connector has a pair of slots that receive opposite edges of the first and second substrates. The channel portions extend across the substrates in a substantially linear path. Each channel portion includes multiple conductors having lengths that are approximately equal.